

### **BSI Standards Publication**

# Integrated circuits - Three dimensional integrated circuits

Part 2: Alignment of stacked dies having fine pitch interconnect



BS IEC 63011-2:2018 BRITISH STANDARD

#### National foreword

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The UK participation in its preparation was entrusted to Technical Committee EPL/47, Semiconductors.

A list of organizations represented on this committee can be obtained on request to its secretary.

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© The British Standards Institution 2019 Published by BSI Standards Limited 2019

ISBN 978 0 580 97375 8

ICS 31.200

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This British Standard was published under the authority of the Standards Policy and Strategy Committee on 31 January 2019.

Amendments/corrigenda issued since publication

Date Text affected



IEC 63011-2

Edition 1.0 2018-11

## INTERNATIONAL STANDARD

## NORME INTERNATIONALE



Integrated circuits – Three dimensional integrated circuits – Part 2: Alignment of stacked dies having fine pitch interconnect

Circuits intégrés – Circuits intégrés tridimensionnels – Partie 2: Alignement de puces empilées à petits pas d'interconnexion

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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ICS 31.200 ISBN 978-2-8322-6291-7

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